Claims

What is claimed is:

1. An isolation circuit for a contact pad coupled to a logic circuit, comprising:

a multiplexer electrically interposed between said contact pad and said logic circuit, wherein said multiplexer is configured to prevent electrical communication between said contact pad and said logic circuit in response to a cut-off signal; and

a drive circuit coupled to said multiplexer and configured to connect to a voltage source and to ground, wherein said drive circuit has a program mode and a non-program mode and is configured to transmit said cut-off signal during said program mode.

2. The isolation circuit in claim 1, wherein said drive circuit further comprises:

a source node;

a signal node coupled to said source node and to said multiplexer;

a fuse coupled to said signal node and having a program function, wherein an initiation of said program function represents a shift into said program mode; and

a ground node coupled to said fuse.

3. The isolation circuit in claim 2 wherein said fuse is selected from a group comprising a laser fuse, a light programmable fuse, and an electrically programmable fuse.

4. A communication device for a logic circuit, comprising:

a logic circuit access terminal;

a connection circuit electrically interposed between said logic circuit and said logic circuit access terminal, wherein said connection circuit is configured to couple said logic circuit to said logic circuit access terminal in response to a coupling signal; and

a signal generation circuit coupled to said connection circuit and configured to receive a voltage source and a grounding pathway, wherein said signal generation circuit has a non-isolation mode and an isolation mode and said signal generation circuit is configured to transmit said coupling signal during said non-isolation mode.

5. The device in claim 4, wherein said signal generation circuit further comprises:

a source node;

a signal node coupled to said source node and to said connection circuit;
an anti-fuse coupled to said signal node; and

a ground node coupled to said anti-fuse, wherein a transmission of said coupling signal through said anti-fuse to said ground node represents a shift into said isolation mode.

6. An isolation circuit for a pathway having a first terminal and a second terminal, comprising:

a first potential node configured to accept a voltage source;

a long L p-channel transistor comprising:

a source coupled to said first potential node, and
a drain;

a signal node coupled to:

said drain of said long L p-channel transistor,

a first conduit, and
a second conduit,

wherein said signal node is configured to receive a signal from said first potential node, and further configured to selectively establish a signal path to said first conduit and to said second conduit;

a signal direction device coupled to said first conduit and having a first mode and a second mode, wherein said signal direction device is configured to maintain said signal path during said first mode, and further configured to change said signal path during said second mode;

a second potential node coupled to said signal direction device and configured to couple to ground;

a connector circuit coupled to said second conduit; and

a multiplexer coupled to said connector circuit and further coupled to said pathway and electrically interposed between said first terminal and said second terminal.

7. The isolation circuit in claim 6, wherein:

said signal node is configured to send said signal through one of said first and second conduits and send a complementary signal through another of said first and second conduits;

said signal direction device is configured to achieve a switch of said signal and said complementary signal with respect to said first and second conduits; and

said multiplexer is configured to electrically separate said first terminal from said second terminal in response to said switch.

8. The isolation circuit in claim 7, wherein said connector circuit comprises:

a first inverter having an input coupled to said signal node and an output coupled to said multiplexer; and

a second inverter having an input coupled to said output of said first inverter, wherein said second inverter also has an output coupled to said multiplexer.

9. The isolation circuit in claim 8, wherein said multiplexer comprises:

a p-channel transistor coupled to said pathway and electrically interposed between said first terminal and said second terminal, wherein said p-channel transistor has a PMOS gate; and

an n-channel transistor coupled to said pathway and to said p-channel transistor, wherein said n-channel transistor is further electrically interposed between said first terminal and said second terminal and has an NMOS gate.

10. The isolation circuit in claim 9, wherein:

said signal direction device is a fuse;

said output of said first inverter is coupled to said NMOS gate; and

said output of said second inverter is coupled to said PMOS gate.

11. The isolation circuit in claim 9, wherein:

said signal direction device is an anti-fuse;

said output of said first inverter is coupled to said PMOS gate; and

said output of said second inverter is coupled to said NMOS gate.

12. A signal regulation device coupled between a first conductive path and a second conductive path, comprising:

a signal reception device configured to carry a first signal having a first voltage and a second signal having a second voltage;

a signal control device coupled to said signal reception device and having an initial mode and an isolation mode, wherein:

said signal control device is configured to accept said first signal and divert said second signal during said initial mode, and

said signal control device is further configured to accept said second signal and divert said first signal during said isolation mode; and

a signal transmission device coupled to said first conductive path, said second conductive path, and to said signal control device, wherein:

said communication device is configured to receive a diverted signal selectively comprising said first signal and said second signal, and

said communication device is configured to allow electrical communication between said first conductive path and said second conductive path in response to receiving said first signal, and said communication device is further configured to prevent said electrical communication in response to receiving said second signal.

13. The signal regulation device in claim 12, wherein said first voltage is higher than said second voltage.

14. The signal regulation device in claim 12, wherein said second voltage is higher than said first voltage.

15. A test mode completion device for a circuit coupled to a redundant contact pad through a test conduit, comprising:

an isolation element, wherein:

said isolation element is incorporated within said test conduit; and

said isolation element is configured to electrically sever said test conduit before said circuit enters a non-test mode.

16. The test mode completion device in claim 15, wherein said isolation element is configured to physically sever said test conduit before said logic circuit enters a non-test mode.

17. The test mode completion device in claim 16, wherein said isolation element comprises a fuse.

18. A test device for an integrated device having a no-connect pin and a die, wherein said die has a logic circuit as well as a test contact pad coupled to said no-connect pin, comprising:

an isolation circuit coupled to said test contact pad and to said logic circuit, wherein said isolation circuit is configured to establish electrical communication between said test contact pad and to said logic circuit in a primary mode and prevent electrical communication between said test contact pad and to said logic circuit in a secondary mode.

19. The test device in claim 18, wherein said isolation circuit is configured to transition from said primary mode to said secondary mode in general correspondence with a transition from a test mode of said integrated device to a non-test mode of said integrated device.

20. A die having logic circuitry and selectively connected to a first group of conductive leads and a second group of conductive leads, comprising:

a first group of contact pads located in a first area on said die, wherein said first area is accessible by said first group of conductive leads;

a second group of contact pads located in a second area on said die, wherein said second area is accessible by said second group of conductive leads; and

an isolation device coupled to said first group of contact pads and to said logic circuitry, wherein said isolation device is configured to regulate electrical communication between said first group of contact pads and said logic circuitry.

21. The die in claim 20, wherein said isolation device is further configured to selectively permanently prevent electrical communication between said first group of contact pads and said logic circuitry.

22. The die in claim 21, wherein:

a prevention of electrical communication between said first group of contact pads and said logic circuitry generally corresponds to an alignment of said second group of contact pads and said second group of conductive leads.

23. The die in claim 22, wherein:

said first group conductive leads are part of a first lead frame; and

said second group of conductive leads are part of a second lead frame.

24. The die in claim 22, wherein said first group conductive leads and said second group of conductive leads are part of a common lead frame.

25. The die in claim 24, wherein a number of contact pads of said first group of contact pads is greater than a number of conductive leads of said first group of conductive leads.

26. The die in claim 25, wherein a number of contact pads of said second group of contact pads is greater than a number of conductive leads of said second group of conductive leads.

27. An adapter for a die having a first and a second contact pad coupled to a logic circuit of said die, wherein said first contact pad is configured to align with a first lead frame and said second contact pad is configured to align with a second lead frame, and wherein said adapter comprises:

a first communication isolator, wherein:

said first communication isolator is electrically inserted between said first contact pad and said logic circuit; and

said first communication isolator is configured to activate generally coincidentally with an alignment between said second contact pad and said second lead frame.

28. The adapter in claim 27, further comprising a second communication isolator, wherein said second communication isolator is electrically inserted between said second contact pad and said logic circuit; and said second communication isolator is configured to activate generally coincidentally with an alignment between said first contact pad and said first lead frame.

29. An isolation circuit for a semiconductor device having a first logic circuit and a second logic circuit, wherein said first logic circuit is coupled to a first contact pad and to a second contact pad, and said second logic circuit is coupled to a third contact pad and to a fourth contact pad, and wherein said isolation circuit comprises:

a program circuit;

a first multiplexer coupled to said program circuit and configured to be selectively driven by said program circuit and further configured to regulate electrical communication to and from one of said first and second logic circuits; and

a second multiplexer coupled to said program circuit and configured to be selectively driven by said program circuit and further configured to regulate electrical communication to and from one of said first and second logic circuits.

30. The isolation circuit in claim 29, wherein said first and second multiplexers are configured to operate concurrently.

31. The isolation circuit in claim 30, wherein said first multiplexer is electrically interposed between said first logic circuit and said first contact pad, and wherein said second multiplexer is electrically interposed between said second logic circuit and said primary contact pad.

32. The isolation circuit in claim 29, wherein said first and second multiplexers are configured to operate selectively.

33. The isolation circuit in claim 32, wherein said first multiplexer is electrically interposed between said first logic circuit and said first contact pad, and wherein said second multiplexer is electrically interposed between said first logic circuit and said second contact pad.

34. A circuit for a plurality of logic circuits respectively coupled to a plurality of contact pads, comprising:

a program circuit configured to have an initial operating characteristic and further configured to optionally permanently transition to a final operating characteristic in response to a reception by said program circuit of a program signal; and

a plurality of multiplexers coupled to said program circuit and respectively electrically interposed between said plurality of logic circuits and said plurality of contact pads, and further configured to deactivate in response to a transition to said final operating characteristic of said program circuit.

35. A selective electrical communication circuit for a logic circuit coupled to a first contact pad and a second contact pad, comprising:

a first multiplexer electrically interposed between said first contact pad and said logic circuit;

a second multiplexer electrically interposed between said second contact pad and said logic circuit and conversely operable in relation to said first multiplexer; and

a program circuit coupled to said first multiplexer and said second multiplexer and configured to drive said first multiplexer and said second multiplexer.

36. The selective electrical communication circuit in claim 35, wherein:

said first multiplexer further comprises:

a first p-channel electrically interposed between said first contact pad and said logic circuit, and

a first n-channel transistor coupled to said first p-channel transistor and electrically interposed between said first contact pad and said logic circuit;

said second multiplexer further comprises:

a second p-channel transistor electrically interposed between said second contact pad and said logic circuit, and

a second n-channel transistor coupled to said second p-channel transistor and electrically interposed between said second contact pad and said logic circuit;

said selective electrical communication circuit further comprises:

a first inverter coupled to said program circuit, to said first n-channel transistor, and to said second p-channel transistor, and

a second inverter coupled to said first inverter, to said first p-channel transistor, and to said second n-channel transistor; and

said program circuit is configured to transmit a first driving signal and further configured to transmit a complementary driving signal in response to a one-time programming event.

37. The selective electrical communication circuit in claim 35, wherein:

said first multiplexer has:

a first communication mode, and

a first non-communication mode;

said second multiplexer has:

a second communication mode concurrent with said first non-communication mode, and

a second non-communication mode concurrent with said first communication mode; and

said program circuit has:

a first operations mode generally concurrent with said first communication mode, and

a second operations mode generally concurrent with said first non-communication mode.

38. A communication regulator circuit for a plurality of logic circuits, comprising:

a first group of multiplexers respectively coupled to said plurality of logic circuits and further configured to allow electrical communication to and from said plurality of logic circuits in response to a reception of a driving signal;

a second group of multiplexers respectively coupled to said plurality of logic circuits and further configured to allow electrical communication to and from said plurality of logic circuits in response to a reception of said driving signal; and

at least one driving circuit coupled to said first group and said second group of multiplexers and configured to initially transmit said driving signal exclusively to said first group of multiplexers and further configured to optionally permanently transmit said driving signal exclusively to said second group of multiplexers.

39. The communication regulator circuit of claim 38 comprising only one driving circuit.

40. The communication regulator circuit of claim 38 comprising a plurality of driving circuits, wherein each driving circuit of said plurality of driving circuits is respectively coupled to a multiplexer in said first group and to a multiplexer in said second group.

41. A testing circuit for a first logic circuit and a second logic circuit, wherein said first logic circuit is coupled to a first main contact pad and a first redundant contact pad, and wherein said second logic circuit is coupled to a second main contact pad and a second redundant contact pad, comprising:

a program circuit configured to transmit a test mode signal before a program event and further configured to transmit a non-test mode signal after said program event;

a first test mode multiplexer coupled to said program circuit, said first logic circuit, and to said first redundant contact pad; and further configured to support electrical communication between said first logic circuit and said first redundant contact pad during a transmission of said test mode signal;

a first non-test mode multiplexer coupled to said program circuit, said first logic circuit, and to said first main contact pad; and further configured to support electrical communication between said first logic circuit and said first main contact pad during a transmission of said non-test mode signal;

a second test mode multiplexer coupled to said program circuit, said second logic circuit, and to said second redundant contact pad; and further configured to support electrical communication between said second logic circuit and said second redundant contact during said transmission of said test mode signal; and

a second non-test mode multiplexer coupled to said program circuit, said second logic circuit, and to said second main contact pad; and further configured to support electrical communication between said second logic circuit and said second main contact pad during said transmission of said non-test mode signal.

42. A method of regulating transmissions between a contact pad and a logic circuit, comprising:

interposing an isolation circuit between said contact pad and said logic circuit;
initially diverting an activation signal from said isolation circuit; and
ultimately directing said activation signal toward said isolation circuit.

43. The method in claim 42, wherein:

initially diverting said activation signal further comprises providing a generally direct path to ground for said activation signal; and

subsequently directing said activation signal further comprises impeding said generally direct path to ground.

44. A method of altering electrical communication between a contact pad and a logic circuit, comprising:

providing an electrical communication circuit between said contact pad and said logic circuit;

initially directing an activation signal to said electrical communication circuit; and
subsequently diverting said activation signal from said electrical communication circuit.

45. The method in claim 44, wherein:

initially directing said activation signal further comprises obstructing a generally direct path to ground for said activation signal; and

subsequently diverting said activation signal further comprises overcoming an obstruction to said generally direct path to ground.

46. A method of testing a logic circuit connected to a first access device, comprising

connecting a second access device to said logic circuit;

examining said logic circuit through said second access device; and

electrically isolating said second access device from said logic circuit.

47. A method of evaluating a logic circuit through a test node, comprising:

inserting at least one transistor between said test node and said logic circuit;

generating a transistor turn-off signal;

providing a ground communication for said transistor turn-off signal;

testing said logic circuit; and

interfering with said ground communication.

48. The method of claim 47, further comprising providing a transistor communication for said transistor turn-off signal.

49. The method in claim 48, wherein inserting at least one transistor comprises inserting at least one p-channel transistor.

50. A method of evaluating a logic circuit through a test node, comprising:

inserting at least one transistor between said test node and said logic circuit;

generating a transistor turn-on signal;

providing a transistor drive communication for said transistor turn-on signal;

testing said logic circuit; and

interfering with said transistor drive communication.

51. The method in claim 50, wherein interfering with said transistor drive communication comprises providing a ground communication for said transistor turn-on signal.

52. The method in claim 51, wherein inserting at least one transistor comprises inserting at least one n-channel transistor.

53. A method of driving a transmission circuit electrically interposed between a first terminal and a second terminal, comprising:

providing a signal to a first node within said transmission circuit;

diverting said signal to a second node within said transmission circuit; and

preventing electrical communication between said first terminal and said second terminal in response to diverting said signal.

54. The method in claim 53, wherein said first node is a driving node and said second node is an isolation node.

55. The method in claim 54, wherein:

diverting said signal comprises programming a fuse; and

providing a signal comprises providing a logic 0 signal.

56. The method in claim 55, wherein:

diverting said signal comprises programming an anti-fuse; and

providing a signal comprises providing a logic 1 signal.

57. A method of preparing a circuit for non-test use, wherein said circuit is coupled to a main contact pad and a test contact pad, comprising:

providing a separation device between said circuit and said test contact pad; and

triggering said separation device.

58. A method of configuring a die to accommodate a plurality of lead frames, wherein said die has logic circuitry, comprising:

providing access to said logic circuitry through a first group of contact pads on said die, wherein said first group of contact pads corresponds to conductive leads of a first lead frame of said plurality of lead frames;

providing access to said logic circuitry through a second group of contact pads on said die, wherein said second group of contact pads corresponds to conductive leads of a second lead frame of said plurality of lead frames;

selecting one lead frame of said plurality of lead frames for attachment to said die; and

providing an accommodating isolation status of said second group of contact pads.

59. The method in claim 58, wherein providing an accommodating isolation status further comprises isolating said second group of contact pads from said logic circuitry in response to selecting said first lead frame.

60. The method in claim 58 wherein providing an accommodating isolation status further comprises maintaining access to said logic circuitry through said second group of contact pads in response to selecting said second lead frame.

61. The method in claim 58, wherein:

selecting one lead frame further comprises selecting a third lead frame having at least one a first conductive lead corresponding to one of said first group of contact pads and having at least a second conductive lead corresponding to one of said second group of contact pads; and

providing an accommodating isolation status further comprises isolating contact pads of said second group of contact pads that do not correspond to a conductive lead of said third lead frame.

62. A method of preparing a die, comprising:

providing a circuit on said die;

accommodating a first lead frame with a first contact pad;

allowing for access to said circuit through said first contact pad;

accommodating a second lead frame with a second contact pad;

allowing for access to said circuit through said second contact pad;

connecting said die to said first lead frame; and

denying access to said circuit through said second contact pad.

63. A method of controlling a communication device between a contact pad and a logic device, comprising:

sending a first signal to a transmission circuit of said communication device;

activating said transmission circuit with said first signal;

sending a second signal to a programmable circuit of said communication device; and

switching said first and second signals.

64. The method in claim 63, wherein switching said first and second signals comprises:

sending said first signal to said programmable circuit; and

sending said second signal to said transmission circuit.

65. The method in claim 64, further comprising deactivating said transmission circuit with said second signal.

66. The method in claim 65, wherein said programmable circuit has a resistance and switching further comprises changing said resistance of said programmable circuit.

67. The method in claim 65, wherein said programmable circuit has a capacitance and switching further comprises changing said capacitance of said programmable circuit.

68. A method of providing test-mode access for an integrated device having a plurality of pins and a die, wherein said die has a logic circuit, comprising:

establishing a temporary connection between said logic circuit and one pin of said plurality of pins; and

maintaining said temporary connection during a test mode of said die.

69. The method in claim 68, further comprising disabling said temporary connection before a non-test mode begins.

70. The method in claim 69, wherein disabling further comprises disabling said temporary connection after said test mode ends.

71. A method of using a no-connect pin of an integrated device during a test mode, wherein said integrated device includes a logic circuit, comprising:

attaching said no-connect pin to a disconnection circuit;

attaching said disconnection circuit to said logic circuit;

allowing a transmission between said no-connect pin and said logic circuit; and

activating said disconnection circuit.

72. The method in claim 71, wherein activating said disconnection circuit further comprises preventing further transmissions between said no-connect pin and said logic circuit.

73. The method in claim 72, wherein attaching said no-connect pin to said disconnection circuit comprises attaching said no-connect pin to said disconnection circuit through a contact pad.

74. A method of regulating electrical communication with a logic circuit coupled to a first communication terminal and a second communication terminal, comprising:

initially allowing electrical communication between said logic circuit and said first communication terminal and between said logic circuit and said second communication terminal; and

subsequently preventing electrical communication between said logic circuit and said second communication terminal.

75. A method of modifying electrical communication between a logic circuit and first and second communication terminals, comprising:

subjecting electrical communication between said logic circuit and said first communication terminal to a multiplexing function; and

making said multiplexing function dependent upon an operational state of a programming element.

76. A method of regulating electrical communication with a logic circuit coupled to a first communication terminal and a second communication terminal, comprising:

allowing electrical communication between said logic circuit and a selection of said first communication terminal and said second communication terminal; and

optionally changing said selection.

77. The method in claim 76, wherein allowing electrical communication further comprises:

multiplexing electrical communication between said logic circuit and said first communication terminal; and

conversely multiplexing electrical communication between said logic circuit and said second communication terminal.

78. The method in claim 76, wherein optionally changing said selection comprises providing for oppositely multiplexing electrical communication between said logic circuit and said first communication terminal and between said logic circuit and said second communication terminal.

79. A method of configuring a die to accommodate a first lead frame and a second lead frame, comprising:

providing a first group of contact pads on said die, wherein said first group of contact pads generally corresponds to conductive leads of said first lead frame;

providing a second group of contact pads on said die, wherein said second group of contact pads generally corresponds to conductive leads of said second lead frame;

providing one of said first and second lead frames for use with said die; and

isolating one group of said first and second groups of contact pads, wherein said one group does not correspond to a provided lead frame.

80. The method in claim 79, wherein:

said method further comprises:

configuring said first group of contact pads to couple to logic circuitry on said die, and

configuring said second group of contact pads to couple to said logic circuitry on said die; and

isolating further comprises restricting electrical communication between said logic circuitry and said one group.

81. The method in claim 80, wherein restricting electrical communication between said logic circuitry and said one group further comprises:

providing a programmable element on said die, wherein said programmable element has a pre-programmed state and a post-programmed state;

making restricted electrical communication between said logic circuitry and said one group dependent upon one state from said pre-programmed state and said post-programmed state; and

providing said one state.

82. The method in claim 81, wherein:

making restricted electrical communication between said logic circuitry and said one group dependent upon one state of said programmable element further comprises making restricted electrical communication between said logic circuitry and said one group dependent upon said pre-programmed state of said programmable element; and

providing said one state comprises maintaining said pre-programmed state.

83. The method in claim 81, wherein:

making restricted electrical communication between said logic circuitry and said one group dependent upon one state of said programmable element further comprises making restricted electrical communication between said logic circuitry and said one group dependent upon said post-programmed state of said programmable element; and

providing said one state comprises programming said programmable element.

84. A method accommodating a first lead frame and a second lead frame with a die, comprising:

providing a first group of contact pads on said die, wherein said first group has a first isolation state and is compatible with said first lead frame;

providing a second group of contact pads on said die, wherein said second group has a second isolation state and is compatible with said second lead frame;

providing one programmable element on said die having an initial operations state and a subsequent operations state;

associating said first isolation state of all contact pads in said first group with said initial operations state; and

associating said second isolation state of all contact pads in said second group with said subsequent operations state.

85. The method in claim 84, further comprising:

selecting said first lead frame for use with said die; and

transitioning to said subsequent operations state.

86. The method in claim 85, wherein transitioning further comprises programming said programmable element.

87. The method in claim 84, further comprising:

selecting said second lead frame for use with said die; and

maintaining said initial operations state.

88. The method in claim 87, wherein maintaining further comprises retaining a configuration of said programmable element.

89. A method of accommodating a plurality of lead frames with a die having logic circuitry, comprising:

providing a first group of contact pads on said die;

providing a second group of contact pads on said die;

providing a plurality of programmable elements on said die, wherein each programmable element of said plurality of programmable elements has an initial operations state and a subsequent operations state;

coupling each programmable element of said plurality of programmable elements to two contact pads, wherein one contact pad is a first group contact pad and another contact pad is a second group contact pad;

isolating one of said two contact pads for each programmable element during said initial operations state; and

isolating another of said two contact pads for each programmable element in response to a transition to said subsequent operations state.

90. The method in claim 89, further comprising:

selecting a lead frame from said plurality of lead frames for use with said die;

transitioning to said subsequent operations state for generally every programmable element having an isolated contact pad corresponding to a conductive lead of said lead frame; and

retaining said initial operations state for generally every programmable element having an isolated contact pad failing to correspond to a conductive lead of said lead frame.

91. The method in claim 90, wherein transitioning further comprises permanently transitioning to said subsequent operations state.

92. The method in claim 91, wherein:

isolating one contact pad of said two contact pads for each programmable element further comprises isolating a first group contact pad; and

isolating another contact pad of said two contact pads for each programmable element further comprises isolating a second group contact pad in response to a transition to said subsequent operations state.

93. The method in claim 91, wherein:

transitioning comprises programming generally every programmable element in which said first group contact pad corresponds to a conductive lead of said lead frame; and

retaining comprises refraining from programming generally every programmable element in which said second group contact pad corresponds to a conductive lead of said lead frame.

94. A method of configuring a die to adapt to one of a plurality of lead frames, comprising:

providing a first group of communication terminals on said die;

providing a second group of communication terminals on said die;

selecting a lead frame from said plurality of lead frames; and

isolating communication terminals that do not correspond to a conductive lead of said lead frame.

95. A method of controlling communication with a first logic circuit and a second logic circuit, wherein a first pathway joins a first contact pad and said first logic circuit, a second pathway joins a second contact pad and said first logic circuit, a third pathway joins a third contact pad and said second logic circuit, and a fourth pathway joins a fourth contact pad and said second logic circuit, wherein said method comprises:

multiplexing said first pathway;

multiplexing said third pathway;

commonly initiating a first multiplexed state at said first and third pathways;

allowing electrical communication through any pathway that is in said first multiplexed state;

allowing a one-time common change to a second multiplexed state at said first and third pathways; and

preventing electrical communication through any pathway that is in said second multiplexed state.

96. The method in claim 95, further comprising:

multiplexing said second pathway;

multiplexing said fourth pathway;

commonly initiating said second multiplexed state at said second and fourth pathways; and

commonly establishing said first multiplexed state at said second and fourth pathways in response to said one-time common change.